APPLICATION		REVISION			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	C65	1	**PRELIMINARY RELEASE**	1-31-91	J. PORTER
		A	SPECIFICATION RELEASE PER ECO 910054	4-3-91	R. BUCKS
		B	REVISED PER ECO 910124	4-25-91	R. BUCKS
		C	REVISED PER ECO 910194	6-26-91	R. Bucks

1.0 DESCRIPTION

The CSG4165-F011 is a low cost MFM disk interface. It requires the use of an external 512 byte RAM as a data cache buffer. This interface can perform reads from and writes to MFM formatted diskettes, as well as free-format full track reads and writes. It can also format diskettes. Logic is also provided for timed head stepping and for motor spin-up. The F011 provides for expansion drive interconnect using a serial protocol for control and status signals. It also incorporates an index pulse simulator for drives that do not have an index sensor.

Unlike its predecessors, this revision shall provide

a. Active high local LED output.
b. Correct remote DSKCHG status.
c. Protection of control bits when changing drive selects.
d. IRQ cleared on reset.
e. Blinking of the local LED.
f. Swapping of buffer halves for CPU access.
g. Two new Digital Phase Locked Loop (DPLL) read recovery methods in addition to the original Full Correction (FC) algorithm.
h. Improved capture range in Full Correction.
i. Decoding for external disk registers.
j. A one line to two line active low decoder for external hardware.

1.1 CONFIGURATION

This device shall be configured in a standard 68-pin PLCC package.

1.2 SOURCES

Refer to Approved Vendor List for sources.

COMMODORE P. N.	STATUS
390491-01	NOT USED
390491-02	INACTIVE
390491-03	INACTIVE
390491-04	ACTIVE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES +/- 1 DEGREE
2 PLACE DECIMALS +/- 0.02
3 PLACE DECIMALS +/- 0.010

DRAWN Mike Rivers	DATE	
SYSTEM ENG.	DATE	
TEST ENG	DATE	
COMP. ENG Drew Shannon	DATE	
CIRCUIT ENG. BILL GARDI	DATE	

Commodore

1200 WILSON DRIVE
WEST CHESTER, PA. 19380
(215) 431-9100

TITLE:
IC, LSI, FLOPPY DISK CONTROLLER, GA4165-F011

SIZE	DRAWING NUMBER
A	390491
SCALE	SHEET 1 OF 21

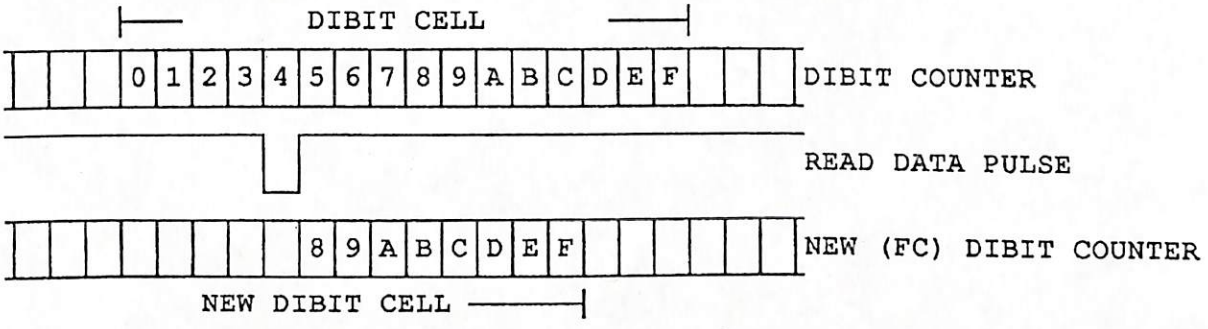
1.3 APPLICABLE DOCUMENTS

Commodore Engineering Policy 1.02.007 Integrated Circuit Qualification Procedure
Commodore Engineering Policy 1.02.008 Integrated Circuit Process Test Specification

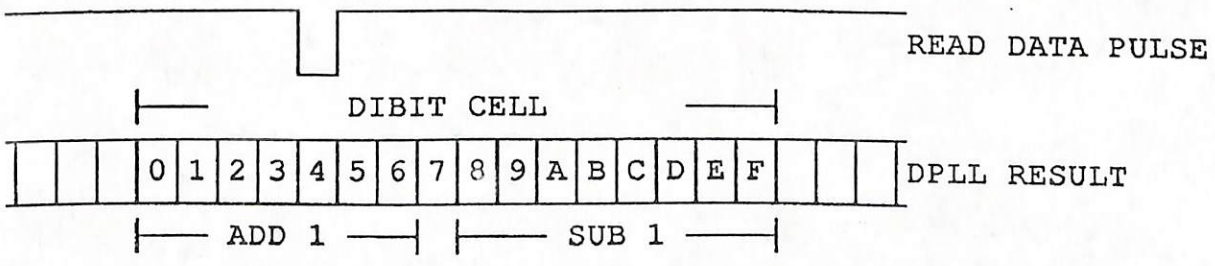
2.0 READ RECOVERY OPTIONS

The F011 now provides 3 methods for recovering MFM formatted disk data. Each method has its own advantages and tradeoffs. This is how they work...

The read-recovery, or dibit counter divides the dibit period into sixteen partitions or counts assuming no read data pulses occur or correctly positioned read pulses occur. When a read data pulse with less-than-ideal positioning occurs, the dibit counter will modify its count depending on whether Full Correction (FC), Digital Phase Locked Loop (DPLL) or Alternate Phase Locked Loop (ALT) recovery methods are selected.



In Full Correction (FC) the dibit counter is forced to count eight after a read pulse is received. This is the equivalent of forcing the read pulse to the center of the bit cell. This method fully compensates for phase and frequency variation. It will tolerate a considerable range of bit frequency error at the cost of permitting a limited range of bit phase error.



In Digital Phase Locked Loop (DPLL) recovery, the dibit counter is incremented if a read pulse occurs early (before a dibit cell center),decremented if a read pulse is late (after a dibit cell center), or counts normally if no read pulse occurs, or if a pulse occurs within a dibit cell center. This method has the ability to track a large range of bit phase error, but, unfortunately can only handle a very narrow frequency error range.

In Alternate Digital Phase Locked Loop (ALT) recovery, the dibit counter behaves exactly as it does in standard DPLL mode, except that if a read pulse occurs more than 3 counts early, or 4 counts late,the counter is incremented or decremented by 2. Like DPLL, this method can tolerate a large range of bit phase error, but can also compensate for a larger frequency error range.

C4165-F011 Pinouts

Pin	Name	Active	Dir	Type	Description
---	-----	------	---	----	-----------
1	RD	low	input	disk	read-data
2	MOT		low	output	disk motor on
3	SIDE		low	output	disk side select
4	WPROT		low	input	disk write protect
5	TK0		low	input	disk track 0
6	WGATE		low	output	disk write gate
7	RW			input	cpu read/write
8	WD		low	output	disk write data
9	A0			input	cpu address
10	A1			input	cpu address
11	A2			input	cpu address
12	A3			input	cpu address
13	INDEX		low	input	disk index
14	GND				
15	D0			I/O	cpu data
16	D1			I/O	cpu data
17	D2			I/O	cpu data
18	D3			I/O	cpu data
19	D4			I/O	cpu data
20	D5			I/O	cpu data
21	D6			I/O	cpu data
22	D7			I/O	cpu data
23	IRQ		low	out oc	cpu interrupt request
24	VCC				
25	VCC				
26	RA8			output	ram address
27	RA7			output	ram address
28	RA6			output	ram address
29	RA5			output	ram address
30	RA4			output	ram address
31	RA3			output	ram address
32	RA2			output	ram address
33	RA1			output	ram address
34	RA0			output	ram address
35	CS		low	input	cpu chip select
36	RRW			output	ram read/write
37	RCS		low	output	ram chip select
38	RD7			I/O	ram data
39	RD6			I/O	ram data

Pin	Name	Active	Dir	Type	Description
40	RD5		I/O	ram	data
41	RD4		I/O	ram	data
42	RD3		I/O	ram	data
43	RD2		I/O	ram	data
44	RD1		I/O	ram	data
45	RD0		I/O	ram	data
46	SERIO	low	I/O	exp	serial control/status
47	LD	low	output	exp	direction of serio
48	CLK	low	output	exp	shift clock
49	LOCAL	low	input	disk	local drive available
50	TSTCLK		input	test	test clock
51	EXTREG	low	output		to external registers
52	A4		input	cpu	address
53	DR0	low	output	disk	drive select 0
54	CS1	low	input	cpu	chip select external logic
55	LED	high	output	disk	panel LED
56	DIR		output	disk	stepping direction
57	STEP	low	output	disk	stepping command
58	PH0		input	cpu	clock
59	DSKIN	low	input	disk	disk inserted
60	RES	low	input	cpu	reset
61	XTAL1		input		crystal
62	XTAL2		output		crystal
63	VENDOR	low	input	vendor	
64	VCC				
65	CSLO	low	output		to external logic
66	CSHI	low	output		to external logic
67	GND				
68	GND				

2.1 SIGNAL DESCRIPTIONS

Processor Interface Lines

A0-A4 — These five address inputs select which internal or external register is to be read or written by the processor.

RW — The RW input determines whether a register will be written (RW=low) or read (RW=high) by the processor.

D0-D7 — Eight bi-directional lines which transfer data to and from the processor during register reads and writes. These are normally inputs, but become driven outputs when CS and PH0 are true.

CS — The Chip Select is a low-true input that determines that a register read or write will occur when PH0 becomes true.

CS1	External hardware chip select input. This low-true signal, when asserted, will cause CSLO to go true (low) if A4 is low, or CSHI to go true (low) if A4 is high.
PH0	A high-true input that must be driven high by the processor to indicate that A0-A4, RW, and CS are valid.
IRQ	The Interrupt Request is an open-drain output that will sink current when an interrupt is requested by the F011C. IRQ will go low (true) when the BUSY status bit changes from true to false if IRQ is enabled.
RES	The Reset is a low-true input used to reset internal events. When RES goes low (true) any command in progress will be terminated. RES will not, however, affect any control register bits.

Buffer RAM Interface Lines

RA0-RA8	These nine RAM Address outputs must be connected directly to nine of the external buffer RAM chip address inputs. These may be scrambled for PCB simplification.
RD0-RD7	These eight bi-directional lines must be connected to the eight bi-directional data lines of the external buffer RAM. These may be scrambled for PCB simplification. RD0-RD7 are inputs except when RRW and RCS are low. Then they become driven outputs.
RRW	The RAM Read/Write output must be connected to the R/W input of the external buffer RAM to control reading and writing.
RCS	The RAM Chip Select is a 1.0 Mhz clock of 50% duty cycle, and is low at a time when RA0-RA8, RRW, and RCS are valid. It must be connected to the CS input of the external buffer RAM.

Disk Drive Interface Lines
(All disk signals are low-true)

RD	The Read Data input expects a series of low-going pulses from the currently selected disk drive.
WD	The Write Data output provides a series of low-going pulses at all times to all drives. It represents the MFM encoded data stream used for disk writes.
WGATE	The Write Gate output, when true, causes the Write Data to be written to the diskette in the currently selected drive.
WPROT	The Write Protect input must indicate, when true, that the present diskette in the local drive must not be written to.

The F011C will not assert WGATE if WPROT is true, and will not execute any write related commands.

LOCAL — The Local Drive Available input must be grouded in systems that have a resident local drive 0, and must be tied to Vcc in systems that are diskless. This will permit drive 0 to be configured externally.

DR0 — This output, when low, indicates that the local drive (Drive 0) is the currently selected drive.

DISKIN — The Disk In Input must indicate when a diskette is physically in the local drive, and the drive is available for use.

MOT — The Motor On output, when true, turns on the motor of the local disk drive only.

LED — The LED output, when true turns on the panel Light-emitting-diode of the local disk drive only.

SIDE — The Side select output determines which side of the media is to be read or written. It is high (false) for side 0, and low (true) for side 1. This output reflects the status of the SIDE control bit regardless of which drive is selected.

STEP — The Step output provides a low-going pulse when a head stepping command is executed, regardless of which drive is selected.

DIR — The Direction output indicates to the drives whether the read/write head is to step toward track 0 (DIR=high) or away from track 0 (DIR=low) when a step pulse is received. This output reflects the status of the DIR command register bit regardless of which drive is selected.

TK0 — The Track Zero input must determine when the read/write head of the local drive is positioned over track zero. This input will not suppress stepping pulses.

INDEX — The Index pulse input must provide a low going pulse for each spindle rotation of the local drive, if the local drive has an index sensor. This input must be tied low if the local drive has no index sensor.

Expansion Drive Interface Lines
(all expansion lines are low-true)

SERIO — The Serial I/O line is a bi-directional signal that is used to pass control to all external disk drives, and to receive

status information from them. It is a driven output when LD is high, and an input, otherwise.

LD — The Load Data output tells the external expansion drives when to update control information shifted off of the SERIO line, when to load status information for shifting, and when to drive the SERIO line. (This is discussed later.)

CLK — The Clock output provides a 50% duty cycle clock at 250Khz to be used by the external expansion drives for shifting control and status information in and out.

Other Signals

XTAL1
XTAL2 — These two lines form two poles of a series-resonant crystal oscillator circuit. XTAL1 is an input, and XTAL2 is an output. An 8.0000Mhz crystal should be used.

VENDOR — The software Vendor identifier input determines whether the F011C will be capable of generating protect marks within the sector headers. Production units will not have this signal bonded, except those shipped to software vendors. This pin should be grounded at all times.

TSTCLK — The Test Clock input is used to reduce F011C test times. This pin should be grounded at all times.

CSLO — External hardware active-low chip select output. Goes low when CS1 and A4 are both low.

CSHI — External hardware active-low chip select output. Goes low when CS1 is low and A4 is high.

EXTREG — External register active-low chip select output. Goes low when CS is low and A4 is high.

C4171-F011C registers

	7	6	5	4	3	2	1	0		
CONTROL	IRQ	LED	MOTOR	SWAP	SIDE	DS2	DS1	DS0	0	RW
COMMAND	WRITE	READ	FREE	STEP	DIR	ALGO	ALT	NOBUF	1	RW
STAT A	BUSY	DRQ	EQ	RNF	CRC	LOST	PROT	TK0	2	R
STAT B	RDREQ	WTREQ	RUN	WGATE	DSKIN	INDEX	IRQ	DSKCHG	3	R
TRACK	T7	T6	T5	T4	T3	T2	T1	T0	4	RW
SECTOR	S7	S6	S5	S4	S3	S2	S1	S0	5	RW
SIDE	S7	S6	S5	S4	S3	S2	S1	S0	6	RW
DATA	D7	D6	D5	D4	D3	D2	D1	D0	7	RW
CLOCK	C7	C6	C5	C4	C3	C2	C1	C0	8	RW
STEP	S7	S6	S5	S4	S3	S2	S1	S0	9	RW
P CODE	P7	P6	P5	P4	P3	P2	P1	P0	A	R

2.2 CONTROL REGISTER

Data from the control register is sent to both the local drive (DR0) and all of the serially connected expansion drives (DR1-DR7). The MOTOR and LED signals will be held for the local drive while other drives are selected.

IRQ — when set, enables interrupts to occur. when reset clears and disables interrupts.

LED — when set, causes LED output to "blink" (alternate between 0 and 1), else see MOTOR, below.

MOTOR — when set, sets the MOTOR output to 0, otherwise 1. Sets the LED output to 1, else 0, unless LED bit is set.

SWAP	swaps upper and lower halves of the data buffer as seen by the CPU.
SIDE	when set, sets the SIDE output to 0, otherwise 1.
DS2-DS0	these three bits select a drive (drive 0 thru drive 7). When DS2-DS0 are zero, DR0 will go true (low) if local is true (low).

Command Register

WRITE	must be set to perform write operations.
READ	must be set for all read operations.
FREE	allows free-format read or write vs formatted
STEP	Causes a head stepping pulse.
DIR	sets head stepping direction
ALGO	selects read and write algorithm. 0=FC read, 1=DPLL read, 0=normal write, 1=precompensated write.
ALT	selects alternate DPLL read recovery method. The ALGO bit must be set for ALT to work.
NOBUF	clears the buffer read/write pointers

2.3 STATUS REGISTERS

The appropriate status bits are sampled from the local status inputs if the local drive (DR0) is selected. Otherwise, those bits are sampled from the serially connected expansion drive.

BUSY	command is being executed
DRQ	disk interface has transferred a byte
EQ	buffer CPU/Disk pointers are equal
RNF	sector not found during formatted write or read
CRC	CRC check failed
LOST	data was lost during transfer
PROT	disk is write protected
TK0	head is positioned over track zero
RDREQ	sector found during formatted read
WTREQ	sector found during formatted write
RUN	indicates successive matches during find operation
WGATE	write gate is on
DSKIN	indicates that a disk is inserted in the drive
INDEX	index is currently over sensor
IRQ	an interrupt has occurred
DSKCHG	indicates that the DSKIN line has changed This is cleared by deselecting drive

Track Register -Sector Register -Side Register

The Track, Side and Sector registers are used in FIND operations to locate a given sector on a given track on a given side.

Data Register

The data register is the CPU gateway to the data buffer for both read and write operations.

Clock Register

The clock register is used to define the clock pattern to be used to write address and data marks. This should be written to FF (hex).

Step Register

The step register is used to time head stepping. This register is compared to a counter, which is clocked at 16Khz, giving a time of 62.5 microseconds per count, allowing a maximum of 16 milliseconds of step time per step operation.

Protect Code Register

The Protection Code register is a read-only register that contains the protect code of the last sector read. If the last sector read does not contain a Protect Mark in its header, then this register will contain zero.

Legal commands are...

hexcode	notes	macro	function
40	1,4,5	RDS	Read Sector
80	1,2	WTS	Write Sector
60	1,4,5	RDT	Read Track
A0	1,2	WTT	Write Track (format)
10	3	STOUT	Head Step Out
14	3	TIME	Time 1 head step interval (no pulse)
18	3	STIN	Head Step In
20	3	SPIN	Wait for motor spin-up
00	3	CAN	Cancel any command in progress
01		CLB	Clear the buffer pointers

Notes:
1. Add 1 for nonbuffered operation.
2. Add 4 for write precompensation
3. Add 1 to clear buffer pointers
4. Add 4 for DPLL recovery instead of FC recovery.
5. Add 6 for Alternate DPLL recovery.

Command Descriptions

Execution of any legal command will cause the BUSY status to be set, and the IRQ, RNF, CRC, and LOST flags to be cleared. Execution of the CANcel or CLearBuffer commands, or any write operation command with the WPROT status set, or any illegal command, will not cause a normal BUSY condition. However, any write to either the Command Register or the Control register will automatically cause BUSY to be set for at least one round trip delay of transmission and reception of the serialized control and status signals. When BUSY gets reset, either by successful command completion, error termination, round trip completion, or by user cancellation, the IRQ flag will be set, and an interrupt generated, unless interrupts are disabled.

The user may CANcel any operation in progress at any time using the CAN command to can it. Use of this command during write operations is not advised.

Unbuffered operations

If the buffer pointers are held clear by setting bit 0 in the command register while issuing a command, unbuffered operations will result. These are most useful for formatting a diskette. The DRQ flag in status register A indicates when a transfer has occurred to or from the disk.

For read operations, DRQ set, indicates that a byte of data has been read from disk, and must be read by the CPU. Reading the data with the CPU will clear the DRQ flag. If the data is not read by the time another byte is read from the disk, the old data will be overwritten and the LOST status flag will be set. The LOST flag will remain set until the next command is written.

For write operations, the user should supply the first byte of data either before, or shortly after issuing a write command. The DRQ flag set indicates that the byte has been written to disk, and the CPU must supply the next byte. When the CPU supplies a byte the DRQ flag will be cleared.

If the CPU does not supply a new byte in the time that it is required by the disk interface, the previous byte data will be written, and the LOST flag will be set. The LOST flag will remain set until the next command is written.

Buffered operations

Buffered operations can be monitored by reading status register A. The DRQ and EQ bits indicate the immediate status of the buffer pointers. During any operation, the EQ bit, when set, indicates that both the disk and CPU buffer pointers are pointing to the same location. This can mean that the buffer is full or empty, depending on what operation is, or will be performed. The DRQ bit set indicates that the disk was last to access the buffer, and clear indicates that CPU was last to access the buffer.

For read operations, the disk interface will read bytes from disk into the buffer. This will set DRQ and clear EQ. The CPU may read data from the buffer at any time after this occurs, and can continue to read data until EQ goes high, indicating that the buffer is empty. CPU reads from the data buffer will clear DRQ. If data is read from disk, setting DRQ, and EQ also gets set, this indicates that the buffer is now full.

One more byte read from disk will set the LOST flag. The LOST flag will remain set until the next command is written. This condition will not usually occur when performing sectored reads of 512 bytes or less, since that is the buffer size.

For write operations, CPU data may be written to the buffer before executing a write command, but may also be supplied during the transfer. If the EQ flag is set after the CPU writes to the buffer, clearing DRQ, this indicates that the buffer is now full, and that the CPU should wait before stuffing more data. If the the EQ flag goes high with DRQ high, this indicates that the disk interface has used all of the available data in the buffer. If one more byte is written to the disk, the LOST flag will be set, indicating old buffer data has been written to disk. The LOST flag will remain set until the next command is written.

Data Transfer Commands

Execution of any of the Data Transfer Commands must be performed assuming that the correct drive has been selected, the proper side has been selected, and the drive's motor is on and has had time to spin up. The read/write head(s) must be positioned over the track that data is to be transferred to or from. If the status of the buffer pointers is not as expected or required, a buffer pointer clear should be performed before writing data or issuing commands.

All write commands should be performed with all bits in the clock register set to a "1" (FF hex). This register is used only for formatting diskettes. For all write operations, the WGATE status flag indicates when data is actually being written to the diskette.

Sectored or formatted operations

These operations differ from free-format commands in that the use of sectors is expected. Sectors are of fixed length, and are located and read or written automatically. The disk control logic will verify that the track/sector/side read from the address marks on the disk match the track/sector/side register contents before transferring any data. If the address marks do not match the address information supplied by the user within 6 index pulses, the command will terminate, BUSY will be reset, and the RNF (record not found) flag will be set. The RNF flag will remain set until the next command is issued. The RUN flag, when set, indicates that so far, the sector being accessed appears to be correct. This flag will reset when any part of the address mark does not match the expected data, or a successful completion occurs. Therefore, RUN can change states several times over a single track.

RDS Read a Sector

Writing a 40 (hex) to the command register will cause the controller to execute a buffered RDS (read sector) command. Writing a 41 (hex) will execute an unbuffered RDS command. Add 4 to either command to select DPLL data recovery instead of the normal FC method. Add 6 to either command to select Alternate DPLL recovery instead of the FC method.

The RDREQ flag, when set, indicates that the requested sector has been found, and is now being read into the buffer. RDREQ will reset after the last byte of the sector is read.

WTS Write a Sector

Writing a 80 (hex) to the command register will execute a buffered WTS (write a sector) command. Add 1 to this command for unbuffered operation, and add 4 if write precompensation is desired. The WTREQ flag, when set, indicates that the requested sector has been found, and is now being written from the buffer. WTREQ will reset after the last byte of the sector is written.

RDT Read a track

Writing a 60 (hex) to the command register will initiate an unformatted buffered disk read. Add 1 to the command for unbuffered operation. Reading will begin immediately, and will continue until user cancellation. The data

recovery logic will use address and data marks to align data to byte boundaries. Add 4 to either command to select DPLL data recovery instead of the normal FC method. Add 6 to either command to select Alternate DPLL recovery instead of the FC method.

WTT Write a track

Writing an A0 (hex) to the command register will initiate a buffered write track operation. Add 1 to this command for unbuffered operation, and add 4 to enable write precompensation.

The Write Track feature is usually only used for formatting diskettes, and will most likely be used in the unbuffered mode, since both data and clock must be supplied on a byte by byte basis. Write normal data with the clock register set to FF hex. Write special marks with missing clocks by writing an FB hex to the clock register.

Writing actually begins with the first index pulse after the command is issued, and continues until the next index pulse.

STIN, STOUT Step In and Step Out

Writing a 10 (hex) or 18 (hex) to the command register will initiate a Step-In or Step-Out operation, respectively. The stepping pulse will be generated immediately, and BUSY will remain set for the duration of the stepping time specified in the STEP register.

Writing a 14 (hex) to the command register will initiate a TIME operation. BUSY will remain set for the duration of the time specified in the STEP register. No stepping pulse will be generated.

SPIN Wait for motor spin-up

Writing a 20 (hex) to the command register will cause BUSY to be set, and stay set for six index pulses. The RNF flag will be set at the end of this operation.

CAN Cancel or "Can" the current operation

Writing a 0 to the command register will force cancellation of any command in progress, and force BUSY to be reset after at least one round-trip serial control and status transmission and reception.

CLB Clear buffer pointers

Writing a 1 to the command register will unconditionally reset the buffer pointers. This should be considered a buffer clear operation, although the contents of the buffer are not affected. The BUSY flag will be set for at least one round-trip serial control and status transmission and reception.

Full Track Writing and
Formatting Diskettes

Writing full-track data and formatting are very similar. Both will require that you generate the appropriate SYNC bytes, so that the read data recovery logic can align the serial bitstream to byte boundaries.

Both descriptions, below, will assume that the spindle motor is on, and up to speed, and that the read/write head is positioned over the track and side to be written.

Track Writes

Full-track writes can be done, either buffered or unbuffered, however, the CLOCK pattern register has no buffer, and writes to this register must be done "one on one".

Write track Buffered

issue "clear buffer" command
write FF hex to clock register
issue "write track buffered" command
write FF hex to data register
wait for first DRQ flag
write A1 hex to data register
write FB hex to clock register
wait for next DRQ flag
write A1 hex to data register
wait for next DRQ flag
write A1 hex to data register
wait for next DRQ flag
write FF hex to clock register
write your first data byte to the data register
you may now use fully buffered operation.

Write Track Unbuffered

write FF hex to clock register
issue "write track unbuffered" command
write FF hex to data register
wait for first DRQ flag
write A1 hex to data register
write FB hex to clock register
wait for next DRQ flag
write A1 hex to data register
wait for next DRQ flag
write A1 hex to data register
wait for next DRQ flag
write FF hex to clock register
loop: write data byte to the data register
check BUSY flag for completion
wait for next DRQ flag
go to loop

Formatting a track

In order to be able to read or write sectored data on a diskette, the diskette MUST be properly formatted. If, for any reason, marks are missing or have improper clocks, track, sector, side, or length information are incorrect, or the CRC bytes are in error, any attempt to perform a sectored read or write operation will terminate with a RNF error.

Formatting a track is simply writing a track with a strictly specified series of bytes. A given track must be divided into an integer number of sectors, which are 128, 256, 512, or 1024 bytes long. Each sector must consist of the following information. All clocks are FF hex, where not specified. Data and clock values are in hexadecimal notation. Fill any left-over bytes in the track with 4E data.

quan	data/clock	description
12	00	gap 3*
3	A1/FB	Marks
	FE	Header mark
	(track)	Track number
	(side)	Side number
	(sector)	Sector number
	(length)	sector Length (0=128,1=256,2=512,3=1024)
2	(crc)	CRC bytes
23	4E	gap 2
12	00	gap 2
3	A1/FB	Marks
	FB	Data mark
128, 256, 512, or 1024	00	Data bytes (consistent with length)
2	(crc)	CRC bytes
24	4E	gap 3*

* you may reduce the size of gap 3 to increase diskette capacity, however the sizes shown are suggested.

Generating the CRC

The CRC is a sixteen bit value that must be generated serially, one bit at a time. Think of it as a 16 bit shift register that is broken in two places. To CRC a byte of data, you must do the following eight times, (once for each bit) beginning with the MSB or bit 7 of the input byte.

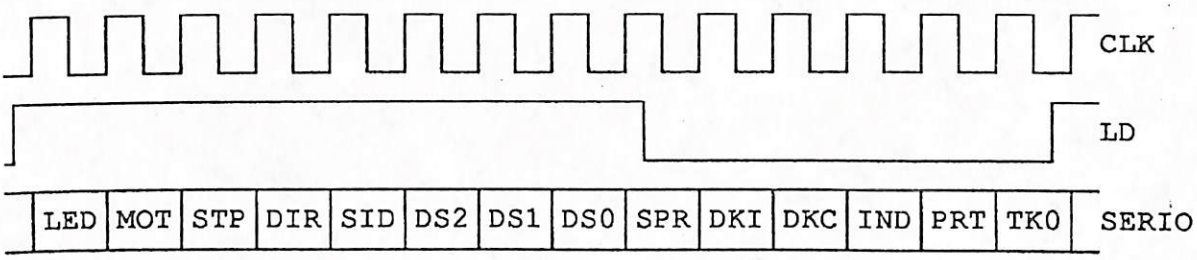
1. Take the exclusive OR of the MSB of the input byte and CRC bit 15. Call this INBIT.
2. Shift the entire 16 bit CRC left (toward MSB) 1 bit position, shifting a 0 into CRC bit 0.
3. If INBIT is a 1, toggle CRC bits 0, 5, and 12.

To Generate a CRC value for a header, or for a data field, you must first initialize the CRC to all 1's (FFFF hex). Be sure to CRC all bytes of the header or data field, beginning with the first of the three A1 marks, and ending with the last byte before the two CRC bytes. Then output the most significant CRC byte (bits 8-15) and then the least significant CRC byte (bits 7-0). You may also CRC the two CRC bytes. If you do, the final CRC value should be 0.

Shown, below is an example of code required to CRC bytes of data.

CRC a byte. Assuming byte to CRC in accumulator and cumulative CRC value in CRC (lsb) and CRC+1 (msb).

```
CRCBYTE     LDX #8          ; CRC eight bits

            STA TEMP

CRCLOOP     ASL TEMP        ; shift bit into carry

            JSR CRCBIT      ; CRC it
            DEX
            BNE CRCLOOP
            RTS

; CRC a bit. Assuming bit to CRC in carry, and cumulative CRC

;           value in CRC (lsb) and CRC+1 (msb).

CRCBIT      ROR

            EOR CRC+1       ; MSB contains INBIT

            PHP
            ASL CRC
            ROL CRC+1       ; shift CRC word
            PLP
            BPL RTS
            LDA CRC                 ; toggle bits 0, 5, and 12 if INBIT is 1.
            EOR #$21
            STA CRC
            LDA CRC+1
            EOR #$10
            STA CRC+1
```



Legend:

Outputs...		Inputs...	
LED	Panel LED On	TK0	Track Zero
MOT	Spindle Motor On	DKI	Disk Inserted
STP	Step Pulse	DKC	Disk Changed
DIR	Step Direction	IND	Index
SID	Side Select	PRT	Write Protect
DS2-DS0	Drive Unit Select SPR	Spare input	

The SERIO pin is bi-directional, and is used for both transmission of drive control signals, and reception of drive status signals. The F011C will drive SERIO when LD is high. The selected remote unit must drive SERIO when LD is low. All SERIO bits are low-true. SERIO will float high for nonexistant drives, making all inputs look false.

All remote units must clock in serial data on the falling edge of CLK. The remote units must update their control information on LD falling if the DS bits match the given unit. All remote units may load their status inputs when LD is high. Remote units shift out serial status on the rising edge of CLK. The F011 will not change LD coincident with CLK, nor will it drive SERIO when LD is changing.

3.0 ELECTRICAL CHARACTERISTICS

3.1 ABOSULTE MAXIMUN RATEINGS

SYMBOL	PARAMETER	MIN	MAX	
VCC	POWER SUPPLY VOLTAGE	-0.5	7.0	VOLTS
VIN	INPUT VOLTAGE	-0.5	VDD+0.5	VOLTS
VOUT	OUTPUT VOLTAGE	-0.5	VDD+0.5	VOLTS
IIN	INPUT CURRENT	100		mA
IOUT	OUTPUT CURRENT	-100	100	mA
TSTG	STORAGE TEMP	-60	150	DEG C.

3.2 D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITONS
VDD	SUPPLY VOLTAGE	4.5	5.5	VOLTS	
Ta	AMBIENT TEMPERATURE	0	70	DEGREE C	
VIL	VOLTAGE IN LOW	VSS-0.3	0.8	VOLTS	TTL
VIL	VOLTAGE IN LOW	VSS-0.3	1.5	VOLTS	CMOS
VIL	VOLTAGE IN LOW	VSS-0.3	0.5	VOLTS	UNBUFFERED
VIL	VOLTAGE IN LOW	VSS-0.3	1.0	VOLTS	BUFFERED
VIH	VOLTAGE IN HIGH	2.0	VDD+0.3	VOLTS	TTL
VIH	VOLTAGE IN HIGH	3.5	VDD+0.3	VOLTS	CMOS
VIH	VOLTAGE IN HIGH	VDD-0.5	VDD+0.3	VOLTS	BUFFERED
VIH	VOLTAGE IN HIGH	4.0	VDD+0.3	VOLTS	UNBUFFERED
IIL	INPUT PULL UP CURRENT	10	50	uA	VIN = 0.4
IIL	INPUT PULLUP CURRENT	10	50	uA	VIN = 2.4
IIH	INPUT PULL DOWN CURRENT	100	250	uA	VIN = 2.4
IIH	INPUT PULL DOWN CURRENT	125	250	uA	VIN = 5.0
IOL	OUTPUT SINK CURRENT	11	22	mA	VOL = 0.4
IOH	OUTPUT SINK CURRENT	13	48	mA	VOH = 2.4
IOH	OUTPUT SINK CURRENT	14	29	mA	VDD-0.5
IOSH	SHORT CIRCUIT HIGH	28	55	mA	VOH = 0.0
IOSL	SHORT CIRCUIT LOW	60	100	mA	VOL = VDD
IIN	INPUT LEAKAGE CURRENT	-10	10	uA	0 < VIN<VD
IOUT	OUTPUT LEAKAGE CURRENT	-10	10	uA	0 <VOUT <VDD

3.3 CELL ASSIGNMENTS

CELL TYPE		PIN NUMBER
TLCH	(TTL)	63
TLCHN	(TTL)	1,4,5,7, 9-13,35,49,50,52,54, 58-61
B1B	(BUFFER)	2, 3, 6, 8, 26-34, 36, 37, 47,48,51,53, 55-57,62,65,66
VSSPAD		14,67,68
BTSE7B	(BUFFER)	15-22, 38-46
TLCHB	(TTL)	15-22, 38-46
B1ODB	(BUFFER)	23
VCCPAD		24, 25, 64

NOTES:

TTL INPUT BUFFERS :	TLCH, TLCB,TLCHI, TLCHN, TLCHBD
CMOS INPUT BUFFERS:	IBUF, IBUFAD, IBUFAU, IBFB, IBUFBD, IBUFBU
SCHMITT INPUTS	SMT1, SMT1B, SMT1D, SMT1D, SMTIBD, SMT1BU
INPUTS WITH PULL UPS	TLCH AND ALL OTHERS ENDING IN "U"
INPUTS WITH PULL DOWNS	ALL INPUTS ENDING IN "D"

Output currents specified for unit buffers. Use the scaling factors below for other sizes

1X	BUFFER	B1, B1OD, B7OD, BTS1,BTS7, BTSE1, BTSE7
2X	BUFFER	B2, B2OD,BTS2,BTS8, BTSE2,B8OD,BTSE8
0.5X	BUFFER	B14,BTS74, B14OD, BTSE14, B74OD, BTS14,BTSE74
0.25X	BUFFER	B18, BTS78, B18OD, B78OD, BTSE18, BTS18,BTSE78

TS = TRISTATE BUFFER
TSE = TRISTATE BUFFER WITH OPPOSITE ENABLE POLARITY
OD = OPEN DRAIN

4.0 PHYSICAL REQUIREMENTS

4.1 MARKING

Parts shall be marked with Manufacturer's Part Number, Manufacturer's Identification, and EIA Date Code. Pin No. 1 shall be identified.

5.0 ENVIRONMENTAL REQUIREMENTS

Units furnished to the requirements of this specification shall meet the following environmental resistance requirements (vendors shall furnish supporting documentation upon request):

Operating Temperature	0 to 70 deg. C
Operating Humidity	5 to 95% RH non-condensing
Operating Altitude	0 to 3000 meters
Storage Temperature	- 20 to + 85 deg. C
Storage Humidity	5 to 95% RH non-condensing
Storage Altitude	0 to 15,000 meters

5.1 PROCESS QUALIFICATION TESTS

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

5.2 ENVIRONMENTAL TEST CONDITIONS

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85 deg. C and 95% RH non-condensing) for 168 hours.
2. Operating life (1000 hours at 70 deg. C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120 deg. C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883,Method 2015, using water and trichloroethane
6. Solder temperature resistance (250 deg. C for five seconds)
7. ESD requirement MIL-STD 1686 Group 3

Note: Devices shall meet this specification's operating performance requirements after the above tests are completed.

5.3 MINIMUM ACCEPTANCE LEVEL

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

5.4 AGE OF DEVICES

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

APPROVED VENDOR LIST

This sheet must be removed from this document before the document is shown or transmitted to a vendor.

Commodore Part Number	Vendor	Vendor Part Number
390491-02 (INACTIVE)	CSG	GA4165-F011B
390491-03 (INACTIVE)	CSG	GA4165-F011C
390491-04	CSG	GA4165-F011D

Commodore			TITLE: IC, LSI, FLOPPY DISK CONTROLLER, GA4165-F011	
SIZE	DRAWING NUMBER: 390491	REV.: C	SCALE	SHEET i OF i